1. A method for implementing a processor-based system comprising:

storing system boot instructions on a programmable, non-volatile memory coupled to a bus which is configured after the boot sequence; and

accessing instructions in the memory in the process of booting the processor-based system.

2. The method of claim 1 wherein storing boot instructions includes storing said instructions on a memory coupled to the peripheral component interconnect bus.

3. The method of claim 1 further including storing an operating system on said non-volatile memory.

4. The method of claim 1 wherein accessing instructions includes using a general purpose output pin on a chipset to supply signals to an A20GATE pin to access the memory during the process of booting the processor-based system.

5. The method of claim 1 wherein storing system boot instructions includes storing the basic input/output system on said memory.

6. The method of claim 1 further including modifying the address of the boot device.

7. The method of claim 6 further including causing a legacy bus controller to ignore said address.

8. The method of claim 8 further including causing a controller associated with said memory to respond to said address.

9. A processor-based system comprising:

a processor;

a volatile memory coupled to said processor;

a peripheral component interconnect bus coupled to said processor; and

a non-volatile memory coupled to said bus storing system boot instructions.

10. The system of claim 9 wherein said system boot instructions include the basic input/output system for said processor-based system.

11. The system of claim 10 wherein said non-volatile memory is a FLASH memory.

12. The system of claim 9 including a chipset coupled to said bus and having a general purpose output pin and an A20GATE pin, the general purpose output pin coupled to said A20GATE pin.

13. The system of claim 12 wherein said A20GATE pin is adapted to create a unique boot address for said non-volatile memory.

14. A memory adapted to be coupled to a peripheral component interconnect bus comprising:

a non-volatile, re-programmable semiconductor memory array storing a basic input/output system; and

a peripheral component interconnect bus controller coupled to said memory array.

15. The memory of claim 14 wherein said memory is a FLASH memory.

16. The memory of claim 13 wherein said controller is configured to respond as the boot device.

17. The memory of claim 13 wherein said controller is not configured to respond as the boot device.

18. The memory of claim 13 wherein said array stores an operating system.

19. The memory of claim 13 wherein said memory is adapted to be re-programmed without user intervention.

20. The memory of claim 13 including a controller adapted to respond as the boot device.